In the Specification:

On page 3, paragraph beginning on line 22 amend as follows:

The intermediate correlation signal and delayed intermediate correlation signals which are derived from every L × N-th tap of shift register 902 are inputted to multipliers 904. The coefficients β_m (m = 1, 2,..., M) of multipliers 904 are determined in accordance with the Search Code with L × M period. Adder ~~904~~903 sums up outputs of multipliers 904 to output the sum thereof as a final correlation signal.

However, the correlation detecting apparatus as shown in FIG. 8 has disadvantages as follows:

A first disadvantage is that shift register 902 is composed of a large number of D-type flip-flops as many as L × (M-1) × N. This causes an increase in circuit scale.

A second disadvantage is that input the data and output data of the D-type flip-flops, as many as L × (M-1) × N, constituting shift register 902 change at each clock tick of the oversampling frequency. This causes an increase in necessitative power consumption.

On page 5, paragraph beginning on line 4 amend as follows:

According to a first aspect of the present invention, there is provided an apparatus for detecting a correlation of samples with a spread code, the samples being obtained by sampling a spectrum spread signal in a range of one symbol period with a oversampling rate which is N-fold of a chip rate, wherein N is an integer larger than zero, the spread code being of L × M period per symbol, wherein L and M are integers larger than one, the spectrum spread signal having been spread in spectrum by the spread code signal, the apparatus comprising: an L-chip accumulator which inputs the samples to generate and output an intermediate correlation signal; M memories ~~as many as M~~, each of which stores L x M samples of the intermediate correlation signal ~~as many as L × N~~; an adder which has M input terminals ~~as many as M~~ and inputs from each of the input terminals the intermediate

correlation signal which is outputted from the L-chip accumulator or the intermediate correlation signal which is outputted from a corresponding memory among the memories; and a controller which supplies the intermediate correlation signal outputted from the L-chip accumulator to the M memories ~~as many as M~~ and to the M input terminals ~~as many as M~~ of the adder in rotation with a unit of L × N samples, and reads, and supplies to each of the input terminals of the adder, the intermediate correlation signal which has been stored in each of the memories M-1 times; wherein an output of the adder is outputted as an correlation signal outputted from the apparatus.

A2 Cont'd

The apparatus may further comprises: M multipliers ~~as many as M~~, each of which is connected with each of the memories and each of the input terminals of the adder; and a coefficient generator which generates coefficients of the multipliers; wherein each of the coefficients changes cyclically in a unit of L × N-fold of a period corresponding to the oversampling rate.

On page 9, paragraph beginning on line 22 amend as follows

A3

An output of L-chip accumulator 101 is inputted to buffers 102-1...102-M. Output lines 103~~7~~-1...103~~7~~-M of buffers 102-1...102-M are connected to data input/output terminals of RAMs 104-1...104-M and first input terminals of multipliers 121-1...121-M, respectively. Output enables of buffers 102-1...102M and output enables of RAMs 104-1...104M are controlled complementarily with interpositions of inverters 103-1...103-M, respectively.

On page 10, paragraph beginning on line 8 amend as follows

A4

Multiplier 121-1 inputs one signal selected from an output of buffer 102-1 and an output of RAM 104-1 by output enable OE1. The same is said of multipliers 121-2...121-M.